



N-Channel 20-V (D-S) 175°C MOSFET

CHARACTERISTICS

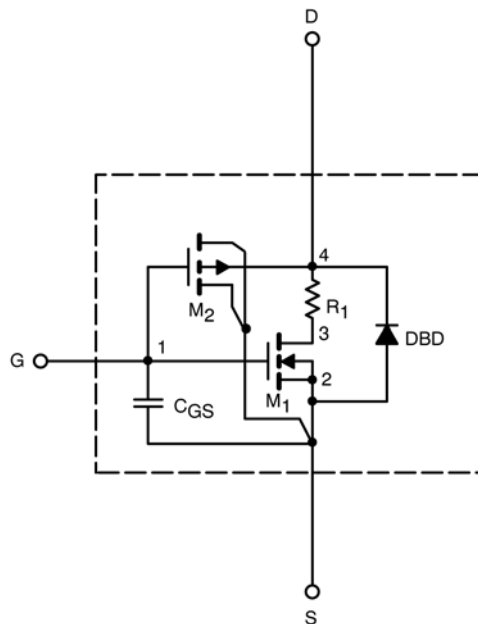
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



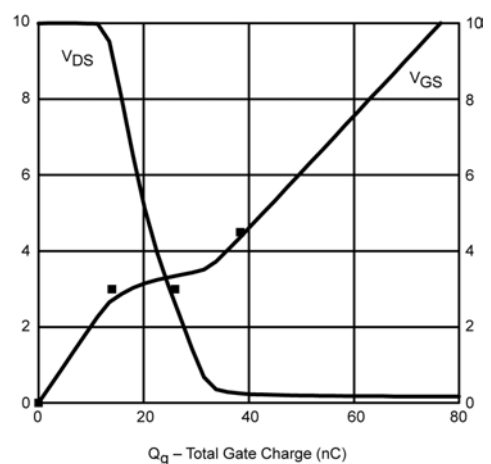
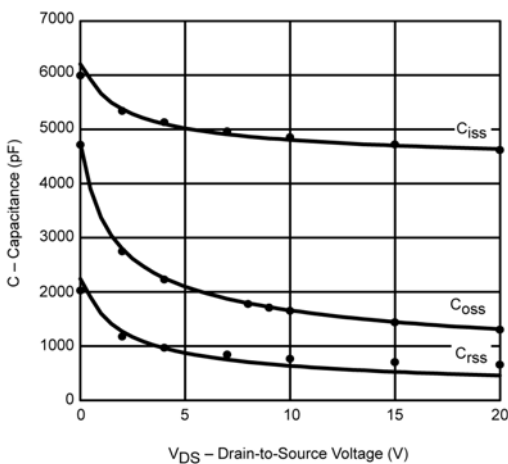
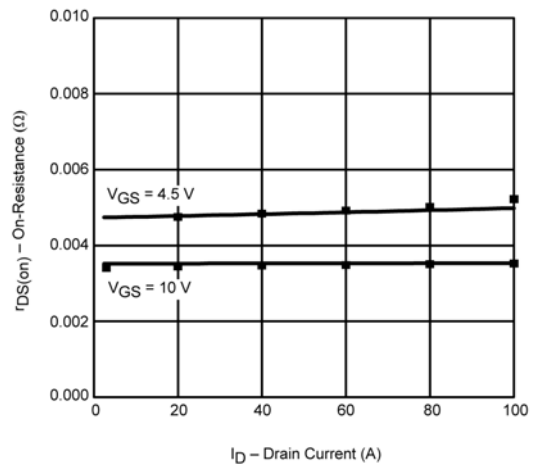
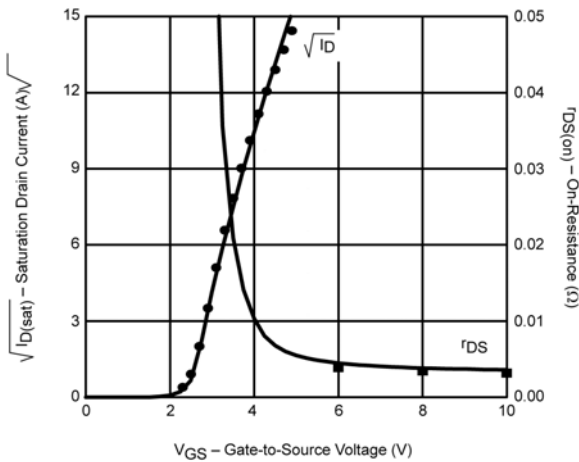
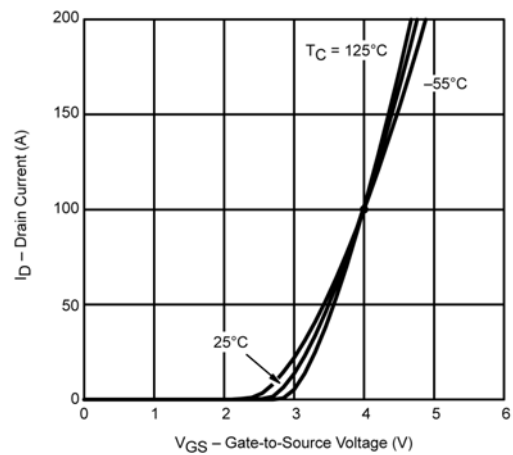
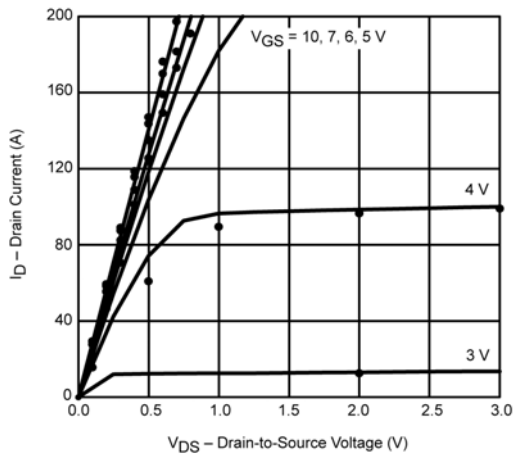
| SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) | | | | | |
|---|--------------|--|----------------|---------------|----------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$ | 1.7 | | V |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$ | 1190 | | A |
| Drain-Source On-State Resistance ^a | $r_{DS(on)}$ | $V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$ | 0.0035 | 0.0035 | Ω |
| | | $V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125^\circ\text{C}$ | 0.0048 | | |
| | | $V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$ | 0.0049 | 0.0048 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15 \text{ V}, I_D = 20 \text{ A}$ | 68 | | S |
| Forward Voltage ^a | V_{SD} | $I_S = 50 \text{ A}, V_{GS} = 0 \text{ V}$ | 0.91 | 0.90 | V |
| Dynamic^b | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0 \text{ V}, V_{DS} = 10 \text{ V}, f = 1 \text{ MHz}$ | 4807 | 5000 | pF |
| Output Capacitance | C_{oss} | | 1664 | 1650 | |
| Reverse Transfer Capacitance | C_{rss} | | 641 | 770 | |
| Total Gate Charge ^c | Q_g | $V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 50 \text{ A}$ | 40 | 40 | nC |
| Gate-Source Charge ^c | Q_{gs} | | 14 | 14 | |
| Gate-Drain Charge ^c | Q_{gd} | | 13 | 13 | |
| Turn-On Delay Time ^c | $t_{d(on)}$ | $V_{DD} = 10 \text{ V}, R_L = 0.20 \Omega$ $I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$ | 31 | 20 | ns |
| Rise Time ^c | t_r | | 18 | 20 | |
| Turn-Off Delay Time ^c | $t_{d(off)}$ | | 34 | 50 | |
| Fall Time ^c | t_f | | 31 | 15 | |

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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